Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor integrated circuit for use in an audio-video device arranged to produce audio-video signals from received encrypted broadcast signals without requiring receipt of one or more transmitted keys, comprising:

an input interface ~~for receipt of a received~~ structured to receive an encrypted enable signal;

an output interface ~~for~~ structured to output ~~of~~ audio-video signals;

one or more hardware circuit portions each ~~arranged~~ structured to process data in relation to the audio-video signals;

a first decryption circuit ~~arranged~~ structured to receive the encrypted enable signal ~~and~~ to decrypt the encrypted enable signal in accordance with a key stored on the integrated circuit and to provide a plain text message ~~and~~ without requiring receipt of one or more transmitted keys;

a memory structured to store ~~containing~~ a stored value for the circuit;

an enabling circuit ~~arranged~~ structured to generate an enable signal or a disable signal to selectively restrict, deny, or allow operation of at least one of the one or more hardware circuit portions;

a common key store structured to store a common key;

a comparison circuit ~~arranged~~ structured to compare the plain text message with the stored value and to selectively instruct the enabling circuit if the plain text message and the stored value match; and

a second decryption circuit ~~in the one or more hardware circuit portions and arranged~~ structured to receive ~~a~~the common key from ~~a~~the common key store in the integrated

circuit and to decrypt the received encrypted broadcast signal in response to receipt of the common key and the generation of the enable signal.

2. (Currently Amended) The semiconductor integrated circuit according to claim 1 wherein the enabling circuit ~~comprises~~ includes one or more switch elements ~~arranged~~ structured to selectively interrupt a data pathway to, from, or within at least one of the one or more of the hardware circuit portions.

3. (Previously Presented) The semiconductor integrated circuit according to claim 2 wherein the data pathway is a critical data pathway, whereby interruption of the pathway prevents operation of the at least one of the one or more hardware circuit portions.

4. (Currently Amended) The semiconductor integrated circuit according to claim 2 wherein the at least one of the one or more hardware circuit portions includes a clock, and the data pathway relates to ~~a~~the clock of the at least one of the one or more hardware circuit portions, whereby the clock is structured to run slower than normal in response to an interruption of the data pathway ~~causes the clock to run slower than normal~~.

5. (Currently Amended) The semiconductor integrated circuit according to claim 4 wherein the at least one of the one or more hardware circuit portions is a main CPU of the semiconductor integrated circuit.

6. (Currently Amended) The semiconductor integrated circuit according to claim 2 wherein the at least one of the one or more hardware circuit portions is a display engine~~,~~ ~~whereby interruption of the data pathway causes~~ structured to cause the video signals at the output interface to be interrupted or impaired in response to interruption of the data pathway.

7. (Currently Amended) The semiconductor integrated circuit according to claim 2 wherein the at least one of the one or more hardware circuit portions is a data port of the

semiconductor integrated circuit that is structured to cease operation in response to~~, whereby~~ interruption of the data pathway ~~prevents operation of the data port~~.

8. (Currently Amended) The semiconductor integrated circuit according to claim 1 wherein the input interface is ~~arranged~~ structured to receive the encrypted enable signal from a broadcast signal.

9. (Currently Amended) The semiconductor integrated circuit according to claim 1 wherein the input interface is ~~arranged~~ structured to receive the encrypted enable signal from a manual input device.

10. (Currently Amended) The semiconductor integrated circuit according to claim 1 wherein the input interface is ~~arranged~~ structured to receive the encrypted enable signal from another device.

11. (Currently Amended) The semiconductor integrated circuit according to claim 1 wherein the enabling circuit ~~comprises~~ includes a store ~~arranged~~ structured to store indications of hardware circuit elements to be restricted, denied, or allowed to operate.

12. (Currently Amended) The semiconductor integrated circuit according to claim 11 wherein the ~~store comprises~~ memory includes one or more hardware fuses.

13. (Currently Amended) The semiconductor integrated circuit according to claim 11 wherein the ~~store comprises~~ memory includes a non-volatile memory.

14. (Currently Amended) The semiconductor integrated circuit according to claim 1 wherein the enabling circuit is ~~arranged~~ structured to extract from the plain text message indications of which hardware circuit elements should be restricted, denied, or allowed to operate.

15. (Currently Amended) The semiconductor integrated circuit according to claim 1 wherein the semiconductor integrated circuit is a monolithic circuit ~~for decryption of broadcast~~ structured to decrypt the audio-video signals.

16. (Currently Amended) The semiconductor integrated circuit according to claim 2 wherein the at least one of the one or more hardware circuit portions ~~relates to storing~~ is structured to store the audio-video signals ~~to~~ on an external storage device, whereby the enabling circuit is ~~arranged~~ structured to selectively restrict, deny, or allow storage of the audio-video signals produced by the circuit.

17. (Currently Amended) The semiconductor integrated circuit according to claim 2, ~~comprising~~ including an input ~~for receiving~~ structured to receive broadcast signals from a broadcast network from which the audio-video signals are produced, and wherein the at least one of the one or more hardware circuit portions ~~relates~~ is structured to ~~production of~~ produce the audio-video signals, whereby the enabling circuit is ~~arranged~~ structured to selectively restrict, deny, or allow production of the audio-video signals.

18. (Currently Amended) A television decoder for encrypted broadcast signals, comprising a semiconductor integrated circuit that ~~comprises~~ includes:

an input interface ~~for receipt of a received~~ structured to receive an encrypted enable signal;

an output interface ~~for~~ structured to output ~~of~~ audio-video signals;

one or more hardware circuit portions each ~~arranged~~ structured to process data in relation to the audio-video signals;

a first decryption circuit ~~arranged~~ structured to receive the encrypted enable signal and to decrypt the encrypted enable signal in accordance with a key stored on the integrated circuit prior to reception of the encrypted broadcast signals and to provide a plain text message without requiring receipt of one or more transmitted keys;

a ~~store containing~~ memory structured to store a stored value for the circuit;

a common key store structured to store a common key;

an enabling circuit ~~arranged~~ structured to generate an enable signal or a disable signal to selectively restrict, deny, or allow operation of at least one of the one or more hardware circuit portions;

a comparison circuit ~~arranged~~ structured to compare the plain text message with the stored value and to selectively instruct the enabling device if the plain text message and stored value match; and

a second decryption circuit in the one or more hardware circuit portions and ~~arranged~~ structured to receive ~~a~~ the common key from ~~a~~ the common key store in the integrated circuit and to decrypt the received encrypted broadcast signal in response to receipt of the common key and the generation of the enable signal.

19-23. (Canceled)

24. (Currently Amended) A circuit for receiving encrypted broadcast signals and producing audio-video signals therefrom, comprising:

a first decryption circuit ~~adapted~~ structured to store a pre-stored key, to decrypt an encrypted enable signal in accordance with ~~a~~ the pre-stored key, ~~that is stored in the first decryption circuit~~ and to output a plain text message without requiring receipt of one or more transmitted keys;

a comparison circuit ~~adapted~~ structured to compare the plain text message with a pre-stored value and to selectively output a control signal if the plain text message matches the pre-stored value; and

a second decryption circuit ~~adapted~~ structured to decrypt the encrypted broadcast signals and produce the audio-video signals in response to receipt of a pre-stored common key and the control signal.

25. (Currently Amended) The circuit of claim 24, comprising an enabling circuit ~~adapted~~ structured to selectively enable, disable, and restrict operation of at least one other circuit in response to the control signal.

26. (Currently Amended) The circuit of claim 25, wherein the enable circuit is ~~adapted~~ structured to select ~~which~~ at least one of a plurality of other circuits in which to selectively enable, disable, and restrict operation in response to the control signal.

27. (Previously Presented) A method of controlling a circuit for receiving encrypted broadcast signals and producing audio-video signals therefrom, comprising:

decrypting an encrypted enable signal in accordance with a pre-stored key without requiring receipt of one or more transmitted keys and to output a plain text message;

comparing the plain text message with a pre-stored value and selectively outputting an enabling control signal if the plain text message matches the pre-stored value; and

decrypting the encrypted broadcast signals and producing the audio-video signals in response to receipt of a pre-stored common key and the enabling control signal.

28. (Currently Amended) The method of claim 27, comprising ~~the further step~~ of selectively enabling, disabling, and restricting operation of at least one other circuit in response to the control signal.

29. (Currently Amended) The method of claim 28, wherein selectively enabling, disabling, and restricting operation ~~comprises~~ includes selecting ~~which~~ at least one of a plurality of other circuits in which to selectively enable, disable, and restrict operation in response to the control signal.

30. (New) The television decoder of claim 18 wherein the enabling circuit includes one or more switch elements structured to selectively interrupt a data pathway to, from, or within at least one of the one or more of the hardware circuit portions.

31. (New) The television decoder of claim 30 wherein the at least one of the one or more hardware circuit portions has a clock that is structured to run slower than normal in response to interruption of the data pathway.

32. (New) The television decoder of claim 31 wherein the at least one of the one or more hardware circuit portions is a main CPU of the semiconductor integrated circuit.

33. (New) The television decoder of claim 30 wherein the at least one of the one or more hardware circuit portions is a display engine structured to cause the video signals at the output interface to be interrupted or impaired in response to interruption of the data pathway.

34. (New) The television decoder of claim 30 wherein the at least one of the one or more hardware circuit portions is a data port of the semiconductor integrated circuit that is structured to cease operation in response to interruption of the data pathway.